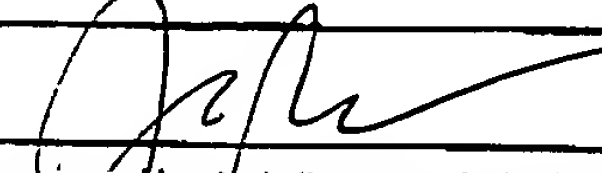


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<b>Substitute for form 1449A/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				Application Number	09/932,330
				Filing Date	August 17, 2001
				First Named Inventor	Jon M. Huppenthath et al.
				Art Unit	2154
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket No.	SRC012

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. <sup>1</sup>	Document No. No. - Kind Code <sup>2</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
JN		US-6,052,134	04/18/2000	Foster	Column 3, lines 12-25; column 5, lines 30 to column 6, line 12; column 6, lines 63 to column 7 line 10.	
JN		US-4,972,457	11/20/1990	O'Sullivan	Column 4, lines 3-12, column 5, lines 50-59; column 7, lines 7-41.	
JN		US-6,452,700 B1	09/17/2002	Mays, Jr.	Column 4, lines 20-42.	
JN		US-5,889,959	03/30/1999	Whittaker et al.	Column 4, lines 42-49.	
JN		US-6,591,157 B1	06/17/2003	Chiles et al.	Column 8, line 66 to column 9 line 8.	
JN		US-6,480,014 B1	11/12/2002	Li et al.	Column 2, lines 47-56.	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>

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ATTY. DOCKET NO. SRC012  
Client/Matter No. 80404.0015

APPLICATION NO.  
09/932,330

INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

FIRST NAMED INVENTOR

Jon M. Huppenthal, Thomas R. Seeman, Lee A. Burton

FILING DATE  
August 17, 2001

ART UNIT  
2154

(Use several sheets if necessary)

Sheet 1 of 1

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Examiner Initials	Cite No.	Document No. No. - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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JN		US-6,052,773	04/18/2000	DeHon et al.	
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FOREIGN PATENT DOCUMENTS

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						YES	NO

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published
JN		YUN, HYUN-KYU AND SILVERMAN, H. F.; "A distributed memory MIMD multi-computer with reconfigurable custom computing capabilities", Brown University, 10-13 Dec. 1997, pp. 7-13.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) Sheet <u>1</u> of <u>1</u>		FIRST NAMED INVENTOR Jon M. Huppenthal, Thomas R. Seeman, Le. A. Burton			
FILING DATE August 17, 2001		ART UNIT 2154			

OCT 11 2002

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U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document No. No. - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JN		US-5,903,771	05/11/1999	Sgro et al.	Figs 1 & 6, col. 3, lines 30-67, col 4, lines 1-51, col 7, lines 1-27.
JN		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
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FOREIGN PATENT DOCUMENTS						
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						YES NO

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published

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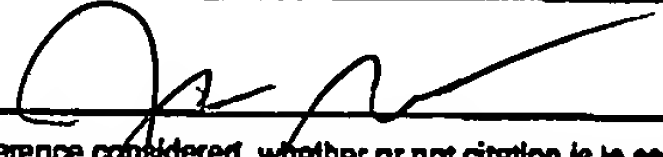
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JW		US-6,581,157 B1	06/17/2003	Chiles et al.	Column 8, line 55 to column 9 line 8.
JW		US-6,480,014 B1	11/12/2002	Li et al.	Column 2, lines 47-56.
		US-			
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Examiner Initials	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
		Country Code <sup>2</sup>	Number <sup>4</sup> Kind Code <sup>5</sup>				

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Sheet 1 of 3

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ATTY. DOCKET NO. SRC0012

SERIAL NO. 09/932,330

INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

APPLICANT: Jon M. HUPPENTHAL, et al.

(Use several sheets if necessary)

FILING DATE: August 17, 2001

GROUP 2154

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLAS S	FILING DATE IF APPROPRIATE
JN	5,230,057	07/20/93	Shido, et al.			
JN	5,892,962	04/06/99	Cloutier			

## FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

	DOCUMENT NUMBER	PUBLISH DATE	COUNTRY	CLASS	SUBCLAS S	TRANSLATION	
						YES	NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JN	AGARWAL, A., et al., "The Raw Compiler Project", pages 1-12, <a href="http://cag-www.lcs.mit.edu/raw">http://cag-www.lcs.mit.edu/raw</a> , Proceedings of the Second SUIF Compiler Workshop, Augs. 21-23, 1997.
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